Improved Flow Control for Minimal Fully Adaptive Routing in 2D Mesh NoC

Alireza Monemi Chia Yee Ooi
Muhammad Nadzir Marsono

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

Maurizio Palesi

University of Enna, Kore, Italy

Oct 2016

Outline

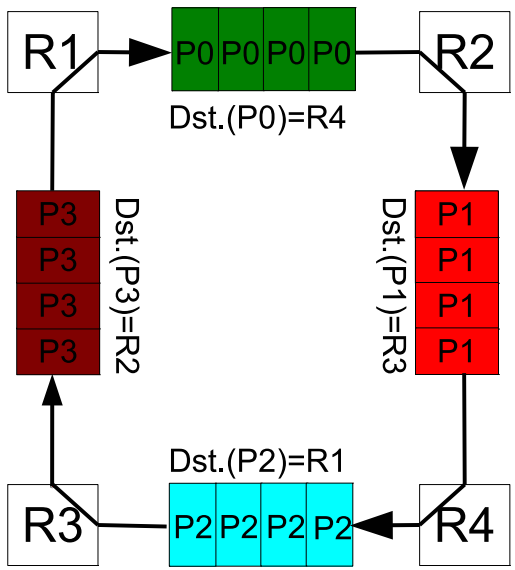
Deterministic Routing

Provides only one specific path for each source-destination IP pair.

- Advantage:
  - Simple architecture when mapped to hardware.
  - Provides high performance when dealing with uniformly distributed traffic.
  - Deadlock free.
- Disadvantage:
  - Results in poor load balancing across all channels for bursty or time variant traffic patterns.

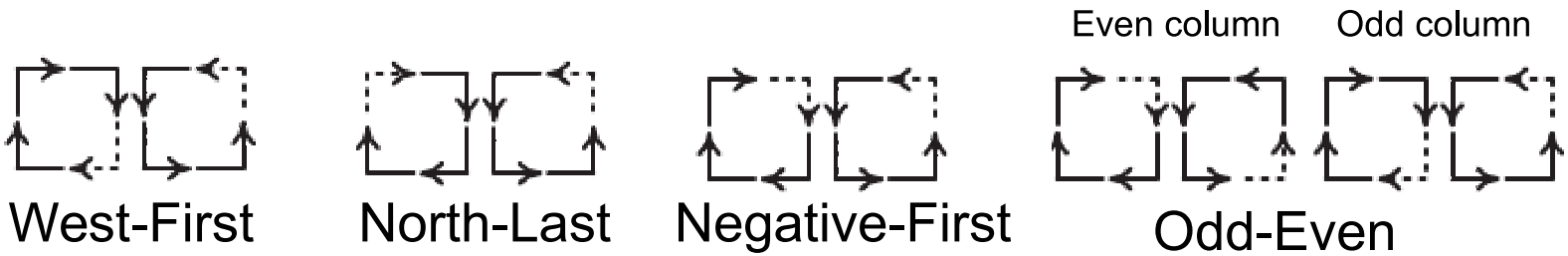
Adaptive Routing

- Adaptive routing allows multiple path selection between a source and destination IP.
- Packets are routed to the path that is less congested.
- Achieves better load balancing.
- Care must be taken in router design to prevent deadlock.
- **Deadlock** happens when several packets are waited for each other's resources in a cyclic order.



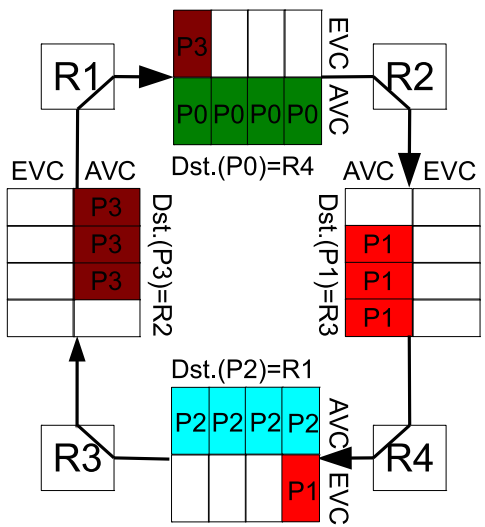
Partially Adaptive Routing

- Deadlock is avoided by prohibiting certain types of turns.
- Results in restriction on the use of certain paths.
- Results in unbalanced adaptivity for different traffic patterns.



Fully Adaptive Routing Based on Duato's Theory [1, 2]

- Separate VCs into two groups: escape VC (EVC) and adaptive VC (AVC).
  (1) EVC: Adhere a deadlock-free routing sub-function (typically DoR).
  (2) AVC: No restriction in routing
- Cyclic dependency can happen in AVCs.
- Packets that do not violate DoR routing can be injected to EVCs and break this dependency.

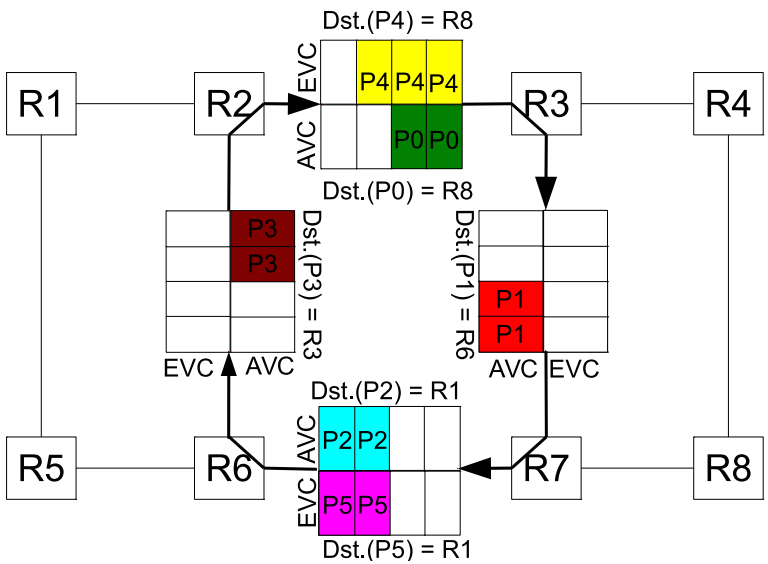


Duato's Theory [1, 2] Restriction #1

(1) Packets are not permitted to switch VC from EVC to AVC.

- Packets that are injected in EVC can only be forwarded via EVCs.
- Once a packet is injected to an EVC, it looses the adaptivity.
- Violating this rules may result in a deadlock condition.

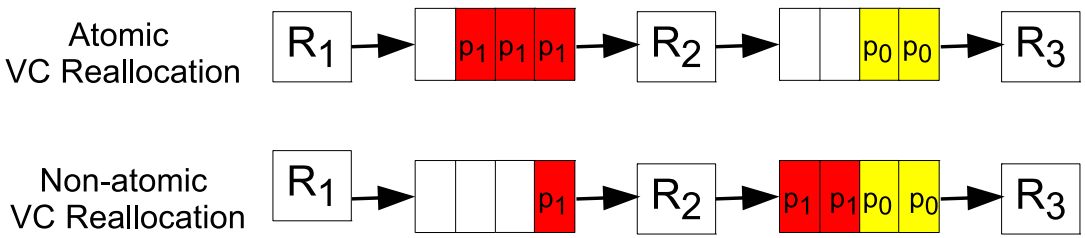
- Deadlock condition example:
  - Assume preferable output ports for all (p_0, p_2, p_4 , p_5) are y dimensions.
  - Due to DoR restriction none of them can be injected to y dimensions' EVCs.
  - p_4, p_5 violates the exchange restriction.
  - Cyclic dependency exist between all packets.



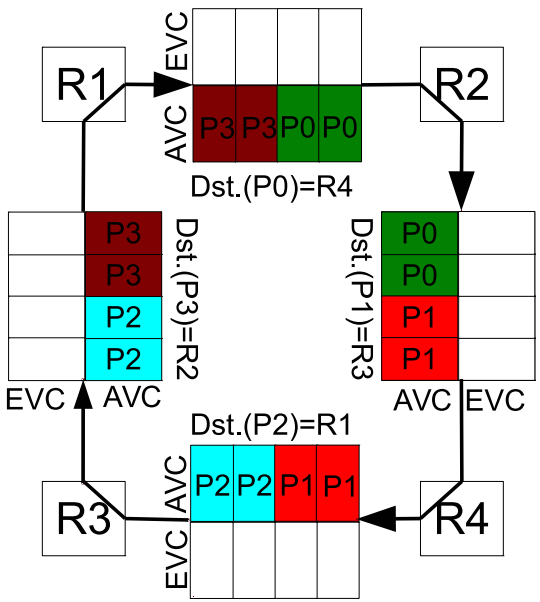
Duato's Theory [1, 2] Restriction #2

(2) Only atomic VC reallocation is supported.

- **Atomic VC reallocation:** Only empty output VC can be reallocated.
- **Non-atomic VC reallocation:** A VC can be reallocated once it receives the tail flit.
- Atomic VC reallocation reduces buffer usage efficiency and increases overall latency.



- Deadlock condition example:

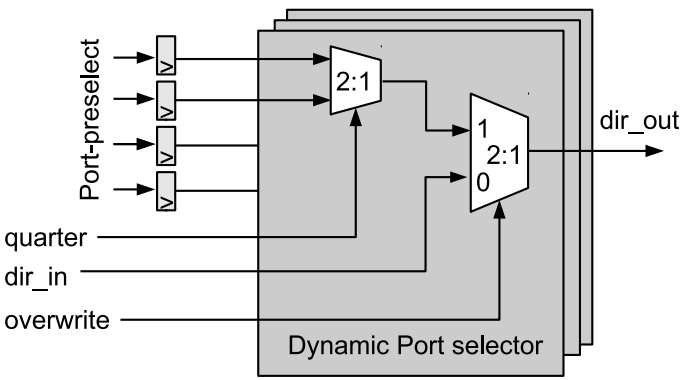


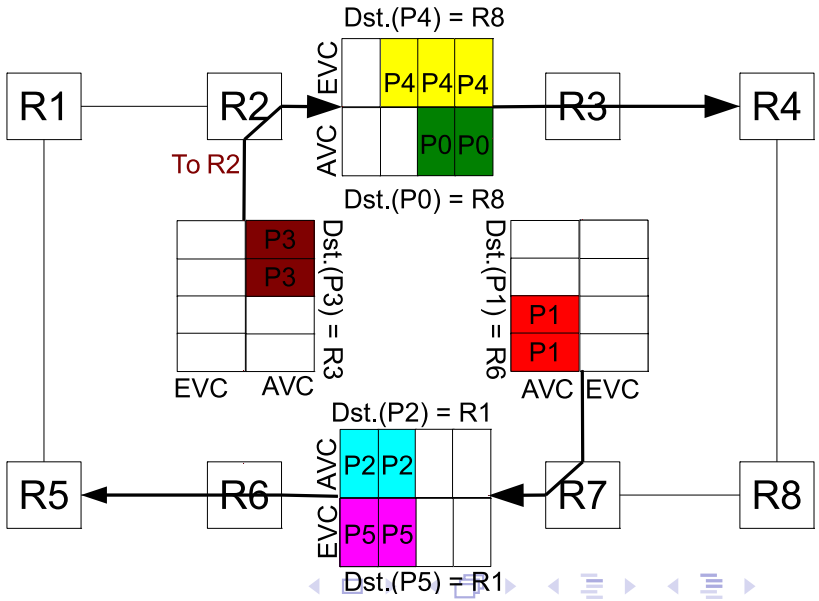
Relaxing Duato's Theory [1, 2] Restrictions

The two aforementioned restrictions can be relaxed in certain conditions [3]:

(1) Exchanging from EVC to AVC is allowed if packets can always request EVCs.
- Solution 1: Send simultaneous VC allocation requests to multiple output ports. This method is **expensive**.
- Solution 2: Use **dynamic port selector** [4, 5] which can swap the requested direction when deadlock happen.

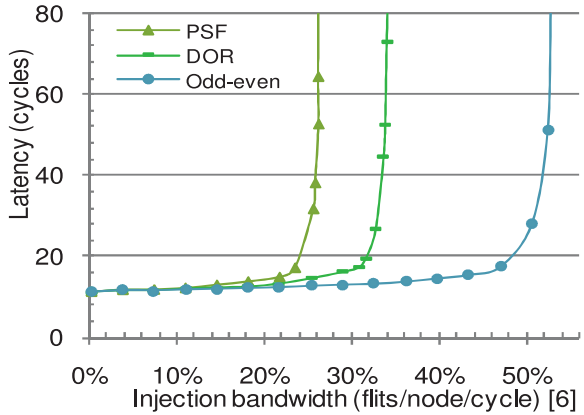
(2) Non-atomic VC reallocation is allowed if in any possible deadlock configuration, at least one packet can have access to an EVC.

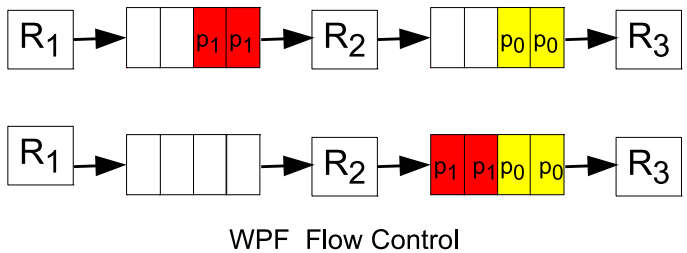




Whole Packet Forwarding (WPF) [6]

- Ma et al. [6] showed fully adaptive routing that has the two aforementioned constraints result in a lower performance compared to DoR and partially adaptive routing with non-atomic VC reallocation support.
- To improve fully adaptive performance, Ma et al. [6] proposed whole packet forwarding (WPF) flow control.
  (1) EVCs can be reallocated non-atomically.
  (2) AVCs can be reallocated non-atomically if they have enough space for storing the whole incoming packet.
- As NoCs' buffer are usually small, WPF is only effective for short sized packets.





WPF Flow Control

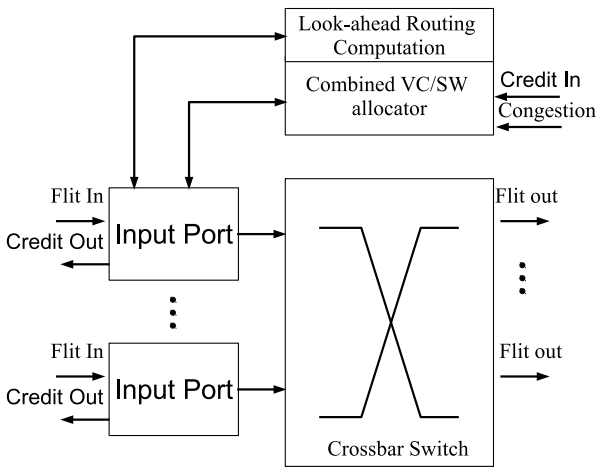
Proposed Minimal Fully Adaptive Routing for 2D Mesh

- Exchange from EVC to AVC is permitted.
- **Atomic VC reallocation** is only required on AVCs located in north and south ports the routers (20% of all available VC).
- **Non-atomic VC reallocation** is allowed on all EVCs and also AVCs located in local, east and west ports of the routers (80% of all VCs).

Reference Design [7]

We have used our previously proposed NoC router in [7] as reference design.

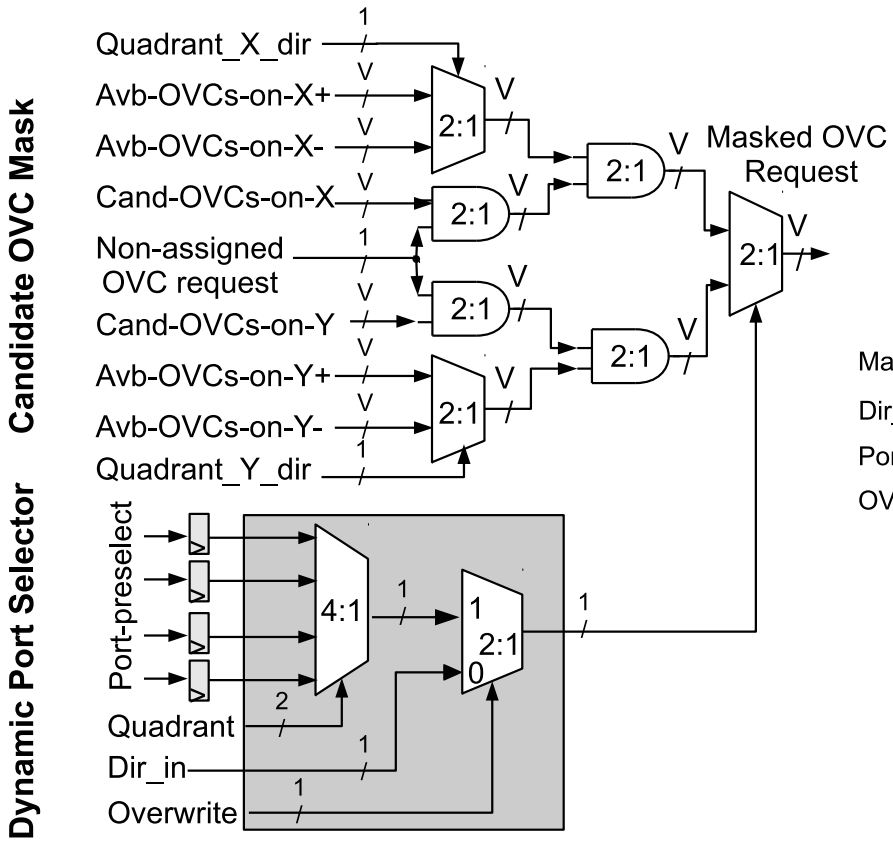
- Optimized for FPGA implementation.
- Support of parameterizable number of VCs, buffer size, flit width and virtual network.
- Speculative or non-speculative combination of VC and switch allocations.
- 2-cycle pipeline latency:
  (1) combined VC/switch allocation and look-ahead routing.
  (2) crossbar traversal.

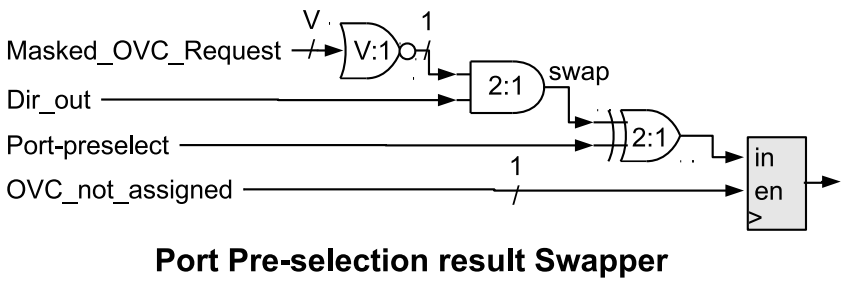


Modification on Reference Design Router

Modification to support exchange from EVC to AVC:

- **Dynamic port selector**: in the case of VC allocation failure, a new optimum output port is selected based on the current state of the network at the beginning of each clock cycle.
- **Port pre-selection result swapper**: swap the pre-selected ports when they are on *y*-dimension but do not have any available AVC.



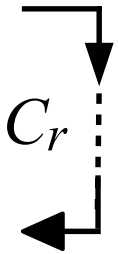


Port Pre-selection result Swapper

Proof of Deadlock Free Routing

Proof using contradiction approach:

- Assume there is a deadlock condition that is created by set of packets $p_1, p_2, p_3, ..p_n$ in a circular path.
- Consider c_r is the rightmost column segment in the channel dependency path.
- Assume packets p_{i-1} and p_i are two packets involved in deadlock condition.
- p_{i-1} is waiting for resources used by p_i.
- p_i is a packet which is using some (or all) resources available in c_r.

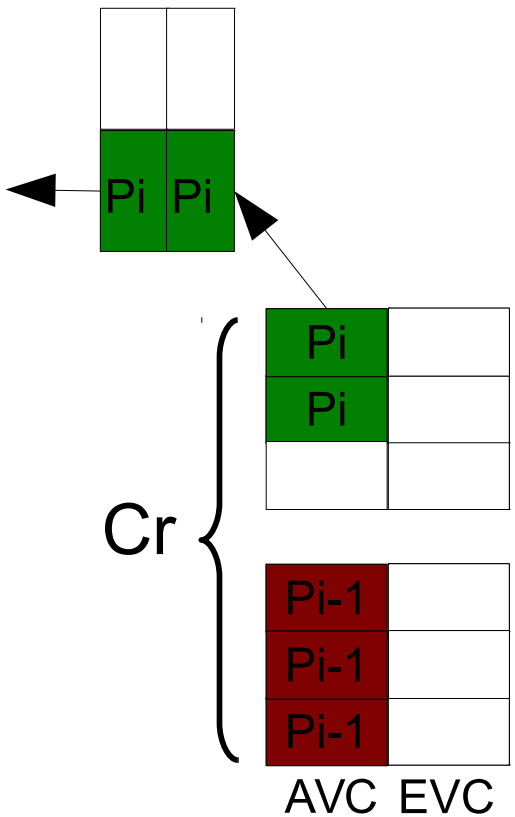


Prove of Deadlock Free

- We will show that in any possible dead lock configuration, at least one of the packets of p_{i-1} or p_i is located at the head head of the queue (VC).
- The proposed dynamic port selection module guarantees that this packet can always be sent to an EVC and break the deadlock condition.
- There are in total three possible conditions which p_{i-1} and p_i can be configured with:

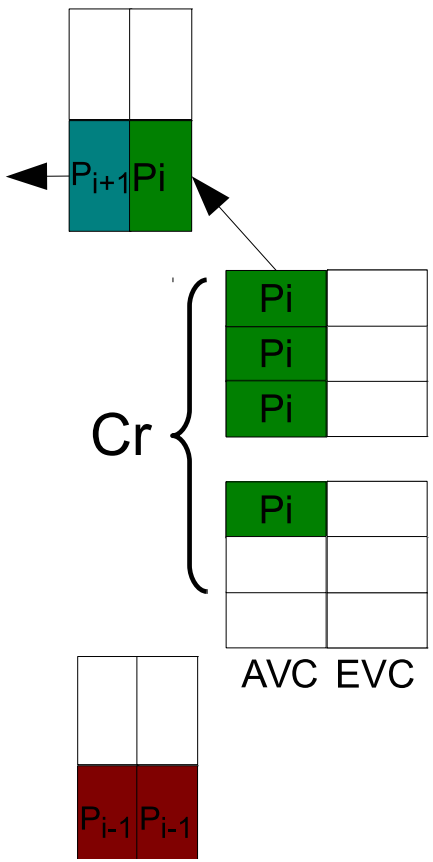
(1) More than one packet are using c_r's resources.

- Let p_i be the last packet that uses the c_r's resources.
- As last packet p_i is involved in turn to the left.
- p_i can not be in EVC as it violates DoR.
- p_i located in AVC which has atomic VC constrain.
- p_{i-1} header flit can not be located in the same VC with p_i tail flit.
- p_{i-1} header flit is in the head of its containing VC.



(2) p_i is the only packet using c_r's resources and its size is smaller than total VCs' buffers located in c_r.

- Similar to previous condition, p_i cannot use any EVCs of c_r
- As the size of p_i is smaller than c_r, the tail of p_i must be located in c_r.
- p_{i-1} which follows p_i is located in another direction (east or west) and is at the head of its queue.



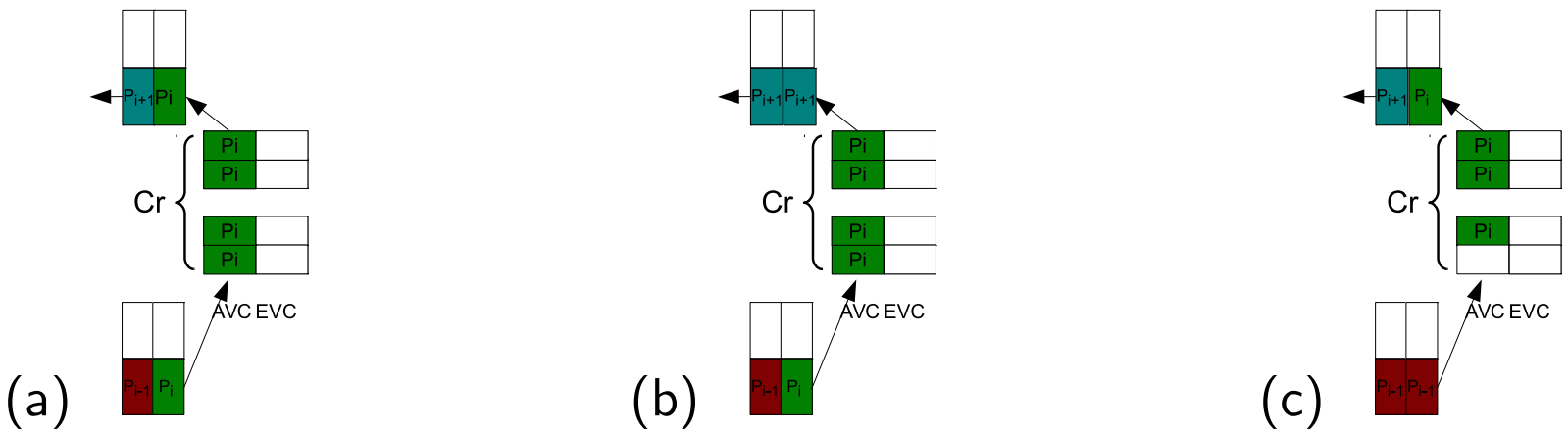
(3) p_i is the only packet that uses c_r's resources and its size is larger than the total buffer size of all VCs located in c_r.

- p_i cannot use any EVC resources of c_r.
- both tail and head of p_i cannot be located in the c_r.
- Here, there are three possible conditions:

  (*a*) None of the head and tail flits are located in c_r. Impossible due to minimal routing.

  (*b*) The head of p_i is located in c_r and its tail is located in another direction. As p_i is the only packet that uses c_r's resources, the head of p_i is located at the head of its queue.

  (*c*) The tail of p_i is located in c_r and its head is located in another direction. As p_i is the only packet that uses the c_r's resources, p_{i-1} which follows p_i is located in another direction and it is at the head of its queue.



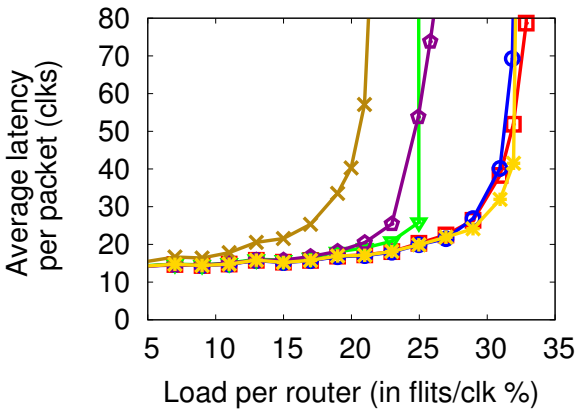
Synthesis Results

Synthesis results summary of different 4×4 NoC configurations configured with 4-VCs per port, flit size of 32 bit and 4-flit buffer size per VC on Stratix IV EP4SGX230KF40C2 Altera FPGA.

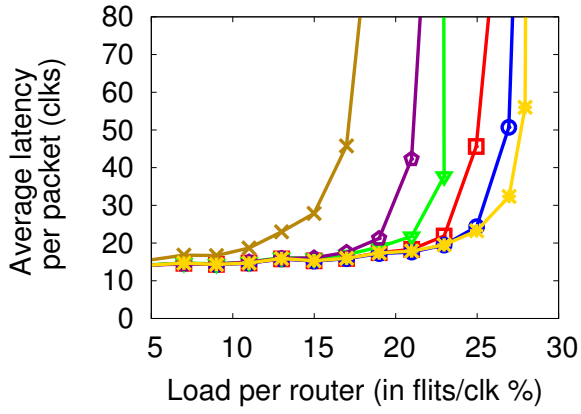
	Deterministic	Fully / partially adaptive
Max frequency	164 MHz	161 -163 MHz
Total BRAM num. (M9k)	64/1,235 (5.2%)	64/1,235 (5.2%)
Total LCU for 4x4 mesh	45,775 / 182,400 (25%)	48,668 - 49,940 / 182,400 (27%)
Average LCU for a 5-port router	3,576 (2%)	3,802 - 3,901 (2%)

- Adaptive NoCs has maximum area overhead of 10% compared to deterministic.
- All different types of NoCs showed similar maximum operating frequencies.

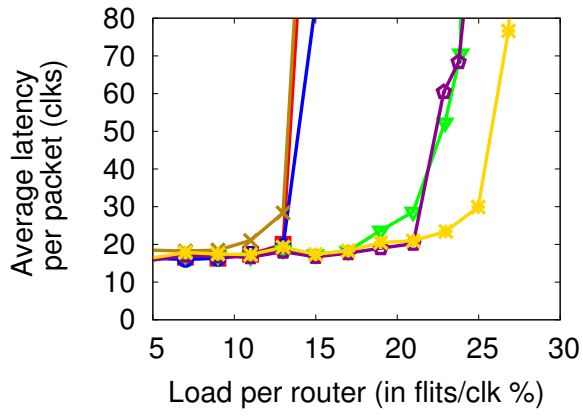
Simulation Results



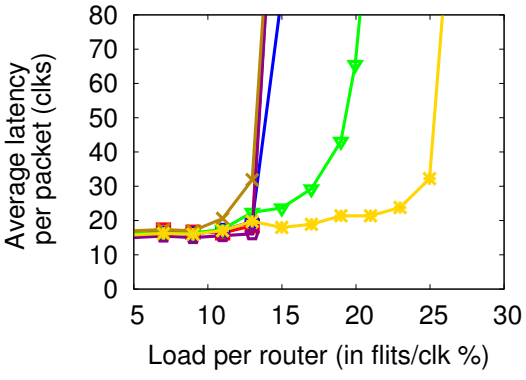
Random.



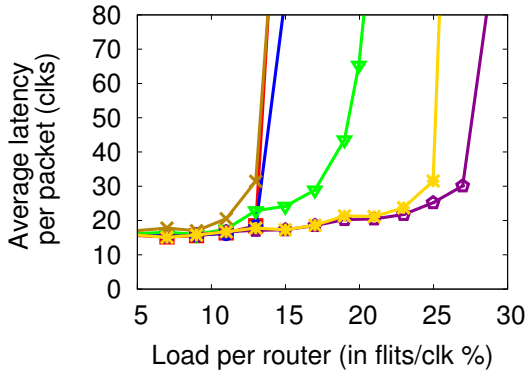
Hot-spot.



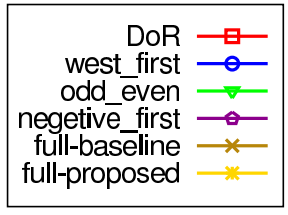
Bit-reverse.



Matrix-transpose-1.



Matrix-transpose-2.



Simulation Results Summary

Average saturation injection rate improvement (on all synthetic traffic patterns) of proposed fully adaptive routing compared to other routings.

Routing algorithm	DoR	West first	Odd even	Negative first	Full baseline
Improvement (%)	58.24	58.85	23.66	29.90	80.60

- The fully adaptive routing with the two mentioned restrictions (full-baseline) shows the worst performance compared to other routing algorithms.
- Negative-first and west-first provide unbalanced adaptivity in the network that result in uneven performance for different traffic patterns.
- Odd-even offers limited adaptivity for unbalanced traffic patterns

Conclusion

- The original Duato's fully adaptive routing [1, 2] restrictions that are atomic VC reallocation and forbidding packets not to switch VC from EVC to AVC result in performance degradation.
- Our proposed dynamic port selection module allows NoC routers to exchange packets from EVCs to AVCs.
- Moreover atomic VC reallocation constrain is only is only compulsory for AVCs which are located in the y dimension of the router in order to have a deadlock-free routing.
- Our proposed fully adaptive router performs better than the baseline Duato's fully adaptive [1, 2] and odd-even partially adaptive routing by providing in average 80% and 24% higher saturation injection load, respectively.

References I

[1] José Duato.
A new theory of deadlock-free adaptive routing in wormhole networks.
IEEE Trans. Parallel Distrib. Syst., 4(12):1320–1331, 1993.

[2] José Duato.
A necessary and sufficient condition for deadlock-free adaptive routing in wormhole networks.
IEEE Trans. Parallel Distrib. Syst., 6(10):1055–1067, 1995.

[3] Jose Duato and Timothy Mark Pinkston.
A general theory for deadlock-free adaptive routing using a mixed set of resources.
IEEE Trans. Parallel Distrib. Syst., 12(12):1219–1235, 2001.

[4] Jongman Kim, Dongkook Park, T. Theocharides, N. Vijaykrishnan, and Chita R. Das.
A low latency router supporting adaptivity for on-chip interconnects.
In *In Proceedings of the 42nd annual conference on Design automation*, pages 559–564, 2005.

[5] Paul Gratz, Boris Grot, and Stephen Keckler.
Regional congestion awareness for load balance in networks-on-chip.
In *High Performance Computer Architecture*, pages 203–214, 2008.

[6] S. Ma, Z. Wang, N. Enright Jerger, L. Shen, and N. Xiao.
Novel flow control for fully adaptive routing in cache-coherent nocs.
IEEE Trans. Parallel Distrib. Syst., PP(99):1–1, 2013.

[7] Alireza Monemi, Chia Yee Ooi, and Muhammad Nadzir Marsono.
Low latency network-on-chip router microarchitecture using request masking technique.
International Journal of Reconfigurable Computing, 2015:2, 2015.